# A VARACTOR BIAS SERVO SYSTEM

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## I. INTRODUCTION

Optimum tuning of varactor multipliers ideally requires a simultaneous adjustment of the varactor bias and several r-f controls, since adjustment of any one control has interacting effects which necessitate readjustment of the other controls. Each control may thus have to be set many times before optimum performance is obtained. A further complication in some varactor circuits (e.g., the balanced doubler described in APP-86 using Fairchild 1N3595 diodes and the multiple stage multiplier string shown in Fig. 1) is that the bias voltages on two varactor diodes must both be controlled at the same time. Since manual tuning of these circuits is tedious and time-consuming, a servo system was built which automatically readjusts the varactor biases to their optimum settings whenever one of the other controls is changed. The design concept is illustrated by the block diagram in Fig. 1.

## II. CIRCUIT OPERATION

To give the servo system maximum operational flexibility, the output d-c amplifiers are operated with independent return lines. Thus the return line

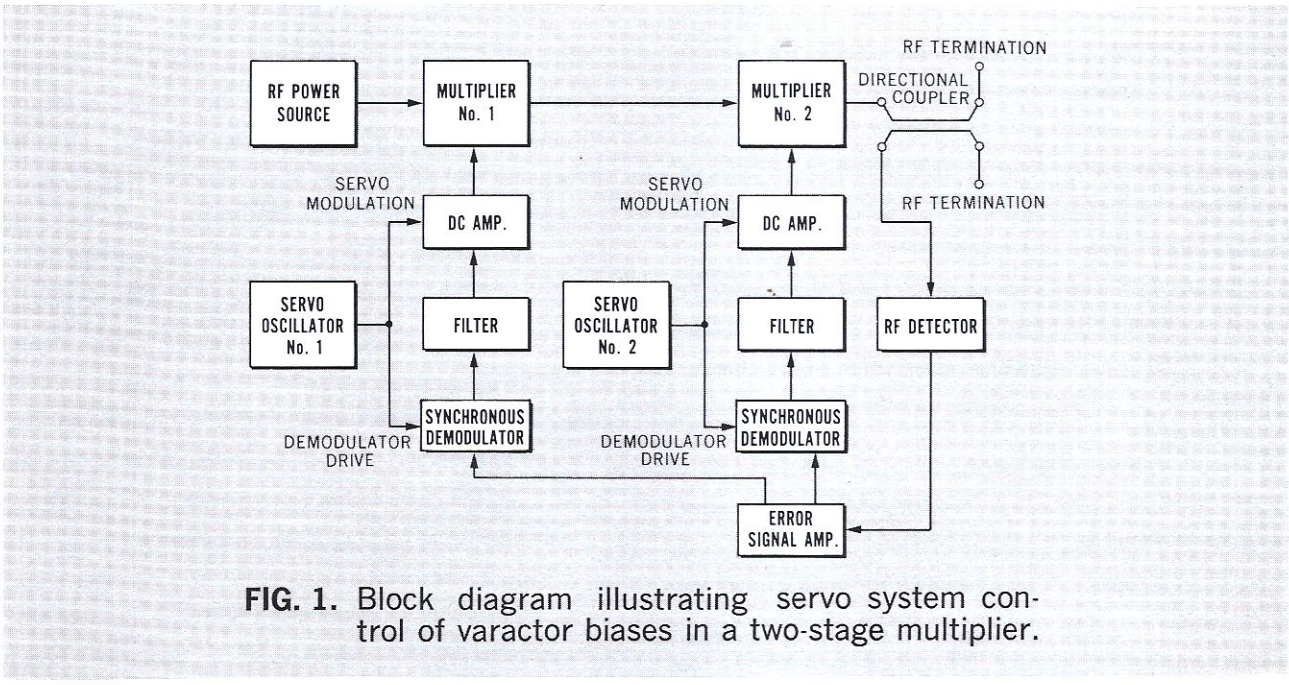


**FIG. 1.** Block diagram illustrating servo system control of varactor biases in a two-stage multiplier.

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of either d-c amplifier may be operated at any potential demanded by the system being controlled. In addition, a fixed power supply can be inserted into the return line, if necessary, to control biases outside the normal range of the servo.

The floating return line was made possible by using a separate d-c to d-c converter to power each d-c amplifier. The complexity of the circuit was reduced by operating each converter at the servo oscillator frequency of its associated servo loop. As may be seen in Fig. 2, the d-c to d-c converters furnish servo modulation, drive the synchronous demodulators, and furnish a-c power to the rectifiers for both positive and negative supplies.

The servo loop operates in the following manner: Each d-c to d-c converter (servo oscillator) adds a small a-c signal, adjusted by the modulation controls, to the output of the d-c amplifier which it powers. The composite signal is applied to the associated varactor as bias and thus slightly modulates the r-f at the servo frequency (see Fig. 3). A sample of the r-f output is fed to a detector and the resultant low-frequency signal contains modulation components of each servo frequency. The phase and magnitude of each component depend upon the direction and magnitude of the adjustment required in the corresponding varactor bias voltage. The entire detector output, including both error signals and any extraneous noise in the system, is amplified in the error-signal amplifier and presented to each synchronous demodulator.

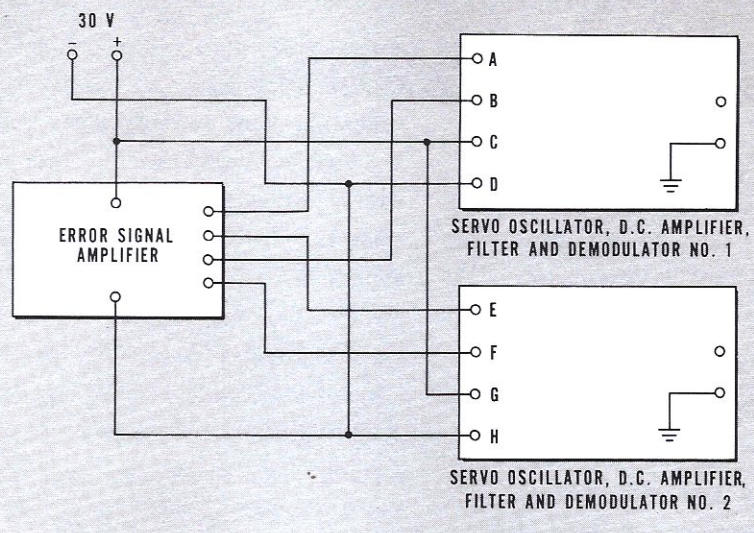
The output of a synchronous demodulator is a complex function of its error signal and reference inputs. The d-c portion of this output (the only portion passed by the filter) is dependent only on the reference signal and that portion of the composite error signal which is synchronous with the reference signal. Thus each demodulator-filter combination converts the error signal into the input signal required by its associated d-c amplifier to deliver the proper bias voltage, and rejects all extraneous signals in the error signal input. A schematic diagram of the complete servo system is shown in Fig. 2.

## III. CIRCUIT DESCRIPTION

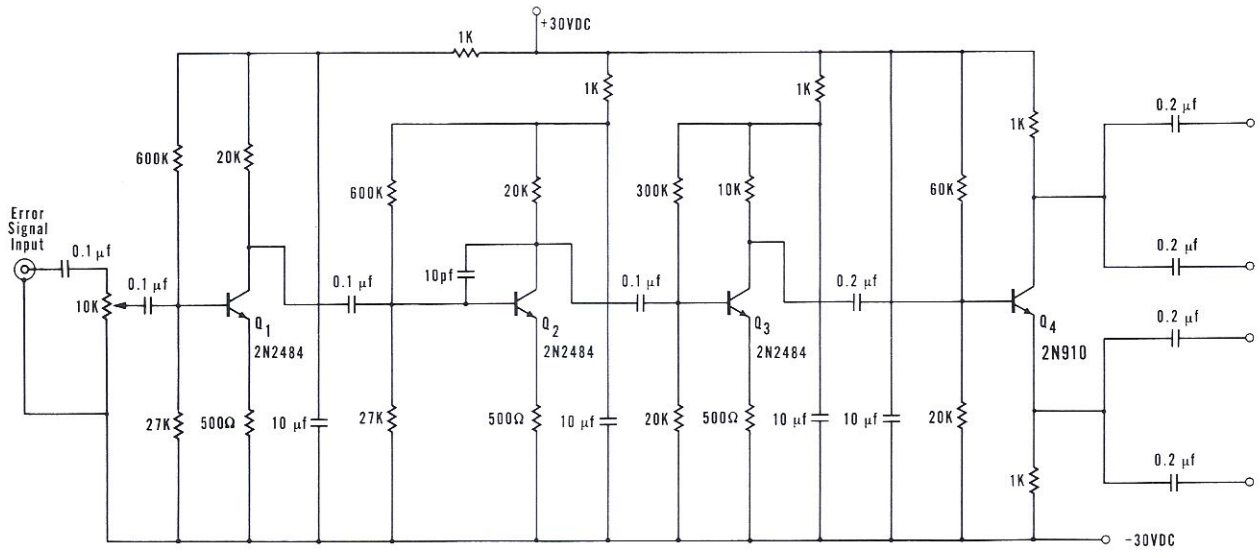
Each d-c amplifier is designed to bias the circuit under test to any point from about -8 V to +28 V with respect to its return line, and to deliver either positive or negative load current at any point within this range. To facilitate this type of operation, a 2N3108 ($Q_{11}$) and a 2N3073 ($Q_{12}$) connected as emitter-followers were used in the output stage, as shown in the schematic (Fig. 2). By using an NPN and a PNP transistor connected between the positive and negative power supplies, it is possible to operate the transistors at low current and hence low dissipation. Also, at any point in the output voltage range, it is possible to accommodate positive load current through one transistor and power supply or negative load current through the other transistor and power supply, depending on the requirements of the circuit under test.

The driver stage consists of a second 2N3073 ($Q_{10}$) connected as a voltage amplifier. It allows conduction in either $Q_{11}$ or $Q_{12}$, depending on the amount and polarity of load current required. A smooth transition from one output transistor to the other is achieved by means of the two FD100 diodes in the collector circuit of $Q_{10}$. When forward-biased by the collector current of $Q_{10}$, these diodes develop a voltage drop very similar in both magnitude and temperature coefficient to the voltage drop across the emitter-base junctions of $Q_{11}$ and $Q_{12}$ (at the threshold of conduction). The 20-ohm resistor in series with these diodes increases the forward bias on the output transistor bases enough to insure that as conduction shifts from one output transistor to the other there will be a slight overlap.

In the preceding stages of the d-c amplifier, PNP and NPN transistors were alternated in order to achieve d-c coupling with a minimum of parts.

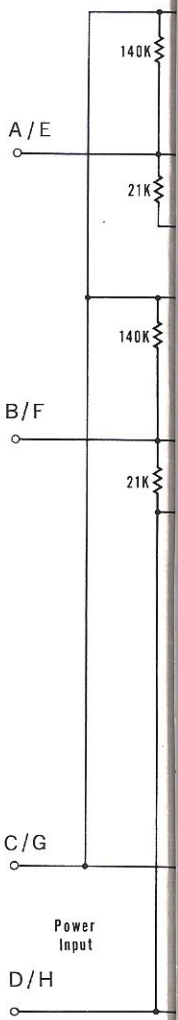



Block Diagram showing connection of Error Signal Amplifier to other units.

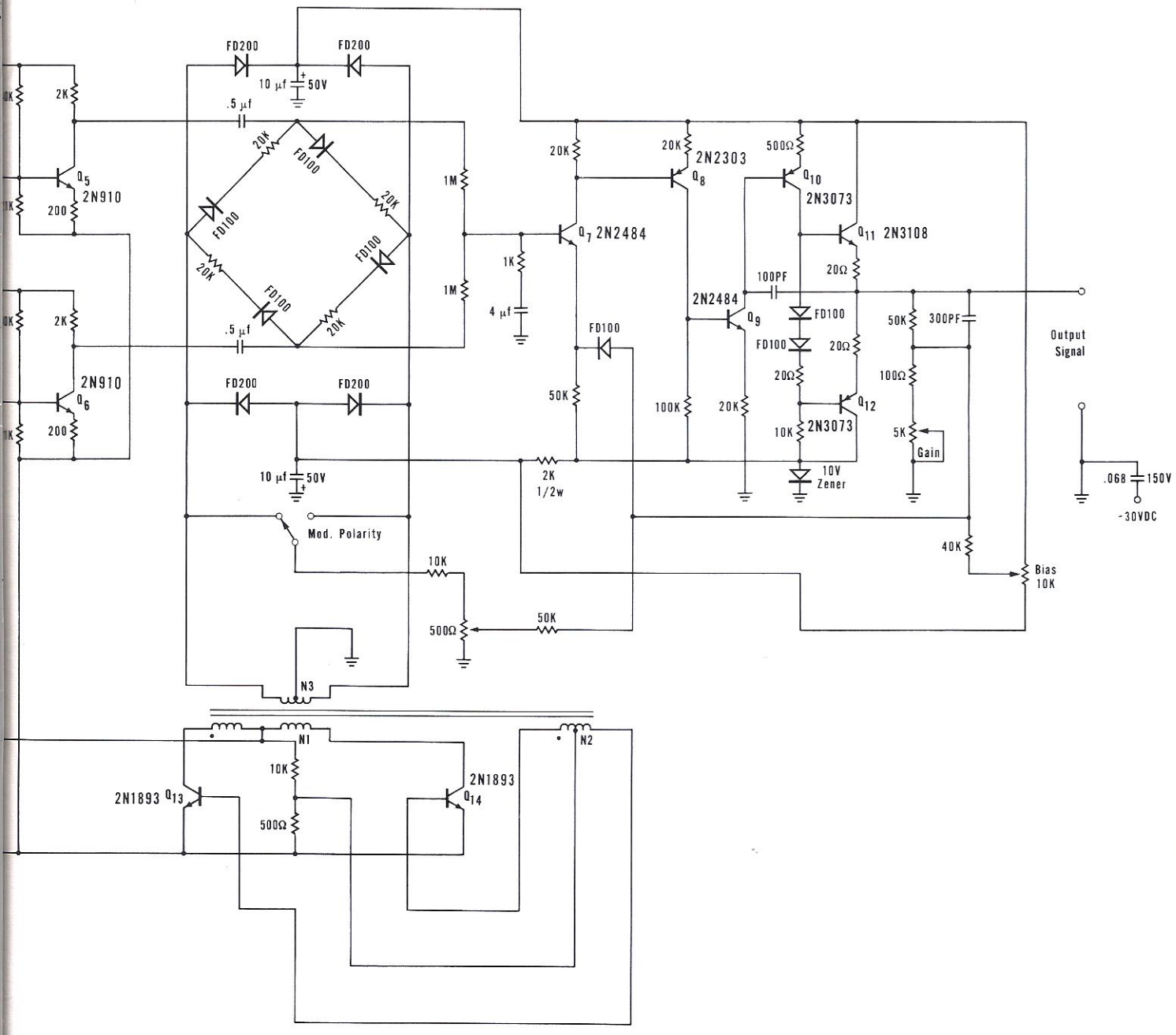



Error Signal Amplifier

FIG. 2. Con



## Complete Schematic of Servo System.




SERVO OSCILLATOR AND D-C AMPLIFIER.
[Units No.1 and No.2 are identical except for transformer specifications.]

TRANSFORMER SPECS:

| | BOARD NO.1 | BOARD NO.2 |
|---|---|---|
| N1 | 150 turns per side | 125 turns per side |
| N2 | 20 turns per side | 18 turns per side |
| N3 | 150 turns per side | 125 turns per side |

The input transistor ($Q_7$), a 2N2484, was selected for its ability to provide high current gain when operated at very low collector current. At the collector current used in this circuit, slightly greater than 0.1 mA, the small signal current gain is typically about 380, and d-c current gain is 175 (min) and 375 (typ).

Gain control is achieved by means of negative feedback applied to the emitter of $Q_7$ through a forward-biased FD100. This diode counterbalances the effect of the emitter-base voltage of $Q_7$ so that when the amplifier is adjusted to give zero output voltage (and hence zero feedback voltage) at zero input signal, the feedback will not affect the amplifier. This condition requires that the feedback be presented to $Q_7$ at its then existing emitter voltage of about -0.6 V, which differs from the feedback voltage by the voltage drop of an FD100 at slight forward current.

The application of the negative feedback to the emitter of $Q_7$ and its high a-c current gain cause the input impedance of the amplifier to be very high, while the high d-c current gain of $Q_7$ at low collector current, and its consequent very small base current, enable the amplifier to operate at a very low quiescent input current. Since these two features of the amplifier permit the use of larger resistors in the filter than would otherwise be possible, the required RC product can be obtained using a capacitor suitable for mounting on a circuit board.

Added to the feedback signal before it is presented to $Q_7$ are:

1. A small sample of the servo oscillator signal, to serve as servo modulation.

2. A d-c bias which can be adjusted to position the zero signal output of the amplifier at any point within its operating range.

Power for the operation of each amplifier is derived from a d-c to d-c converter. The 2N1893 was selected for the oscillator section ($Q_{13}$ and $Q_{14}$) because of its low saturation voltage at the current levels expected in this circuit as well as its ability to withstand the expected peak collector voltage with adequate margin for transients.

The center tap of the transformer secondary winding is connected to the return line of the d-c amplifier, and the positive and negative power-supply voltages are rectified by pairs of FD200 diodes. With this arrangement, the return line of the d-c amplifier can be operated at any desired potential, and the power supply will automatically furnish the correct positive and negative voltages with respect to the amplifier return line. The FD200 was chosen because it can accommodate the d-c current and peak inverse voltage expected in this circuit with adequate safety factor, and because its switching speed is great enough to permit efficient operation of the converter over a wide range of servo oscillator frequencies.

The synchronous demodulator consists of four FD100 diodes and four 20-K resistors. When a balanced a-c input is applied to each of the diagonals of the resistor-diode ring, a d-c potential related only to those a-c components appearing simultaneously in both inputs is developed between the center taps of the a-c sources. In general, the polarity of this potential is dependent on the phase relationship between the a-c signals while its magnitude is dependent primarily on the smaller of the a-c signals. (Detailed explanations of the way this potential is developed can be found in articles on ring modulators, phase detectors, or balanced modulators.)

In this circuit one of the a-c inputs to the synchronous demodulator is supplied by winding N3 of the d-c converter; the other, the composite error signal, is supplied by $Q_5$ and $Q_6$. Thus the d-c output of the demodulator is a function of the error signal component which is synchronous with the reference signal. As can be seen from Fig. 3, the magnitude and phase of this error signal component depend on the magnitude and direction of adjustment

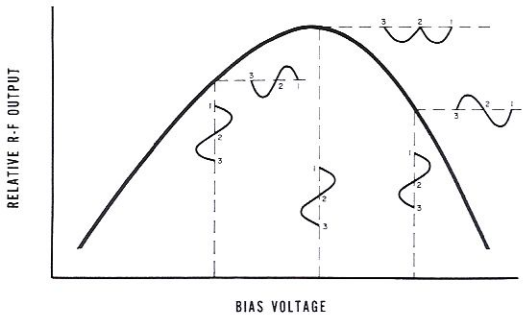



**FIG. 3.** Response of r-f output to varactor bias voltage showing superimposed servo frequency signal.

required in the varactor bias. Thus the demodulator output, after filtering, is the d-c error signal required for bias correction.

The transistors delivering the a-c error signal to the synchronous demodulator ($Q_5$ and $Q_6$) provide the last stage of a-c error signal voltage gain and also provide isolation between the two synchronous demodulators. This isolation is necessary to prevent signals from being transmitted from one synchronous demodulator to the other through the error signal amplifier (see Fig. 1), causing undesirable interchannel reactions. The 2N910 was selected for this stage because it combines the required current and voltage capability with an unusually high current gain and thus assures a sufficiently high load impedance for the phase inverter ($Q_4$)

The first three stages of the error signal amplifier ($Q_1$, $Q_2$, and $Q_3$) take advantage of the high gain and low noise characteristics of the 2N2484. In order to prevent changes of gain or phase shift due to changes in signal level or ambient conditions, each stage is biased to provide a high degree of operating point stability along with considerable a-c emitter degeneration. This stability is necessary because of the possibility that while one channel is resting at its null (very small error signal) the other channel may experience some circuit disturbance, giving rise to extremely large error signals. In order to avoid undesirable interchannel disturbances in situations like this, the amplifier must have stable gain and phase characteristics over a very wide range of signal levels. The low noise figure of the 2N2484 is important to this amplifier because the noise generated in $Q_1$, when amplified by the succeeding stages, must not monopolize an appreciable portion of the output capability of $Q_5$ and $Q_6$.

## IV. SERVO APPLICATIONS

This servo system, originally built to expedite testing of the balanced varactor doubler described in APP-86, has also been used to control the neutralization of r-f transistor amplifiers in automatic test equipment. The flexibility of the design makes it suitable for any system in which automatic d-c control in response to an error signal is possible.